(54) Titre : CIRCUIT DE COMMANDE D'ALIMENTATION POUR L'ELEMENT CHAUFFANT D'UN DISPOSITIF
ELECTROPHOTOGRAPHIQUE
(54) Title: POWER CONTROL CIRCUIT FOR THE HEATING ELEMENT OF AN ELECTROPHOTOGRAPHIC DEVICE
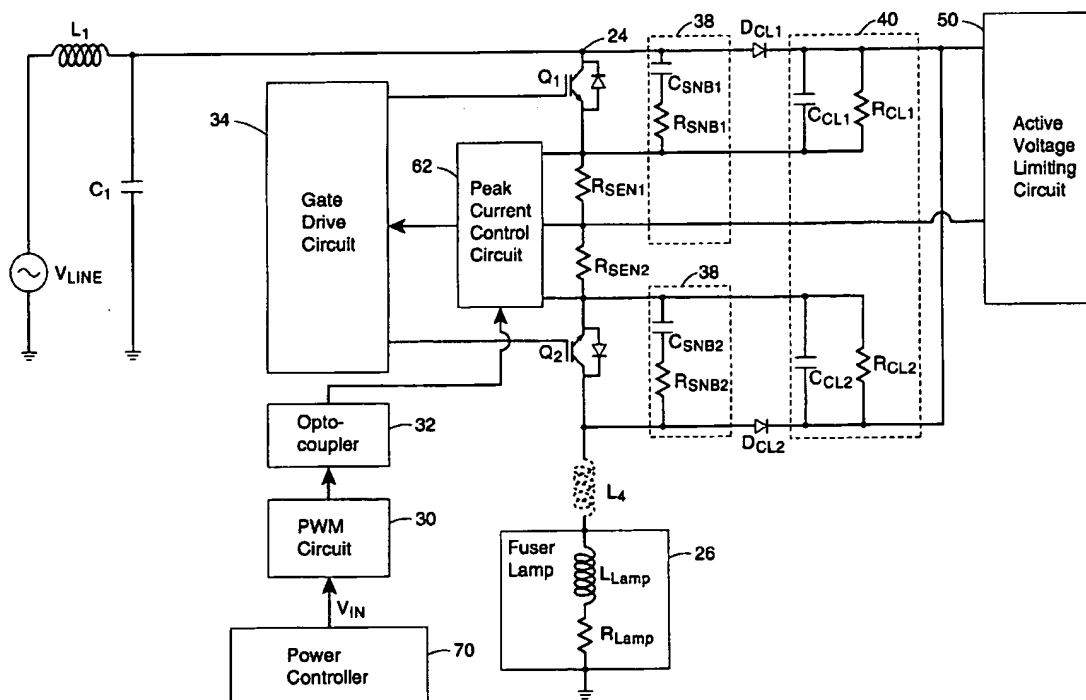
(57) Abrégé/Abstract:
Power control circuitry for regulating power to the heating element of an electrophotographic copier or printer. The circuitry uses
a low pass filter to filter an AC power source and employs a PWM control technique to periodically apply the filtered AC power
through a bi-directional AC switch to the heating element. Snubbing circuitry periodically dissipates the energy accumulated in
the parasitic inductance of the heating element. The parasitic energy is dissipated through a resistance that varies depending on
the amount of energy stored in the parasitic inductance. This minimizes the power loss attributable to the snubbers. The circuitry
also limits EMI and harmonic currents to tolerable levels, and enables flicker to be controlled.

ABSTRACT

Power control circuitry for regulating power to the heating element of an electrophotographic copier or printer. The circuitry uses a low pass filter to filter an AC power source and employs a PWM control technique to periodically apply the filtered AC power through a bi-directional AC switch to the heating element. Snubbing circuitry periodically dissipates the energy accumulated in the parasitic inductance of the heating element. The parasitic energy is dissipated through a resistance that varies depending on the amount of energy stored in the parasitic inductance. This minimizes the power loss attributable to the snubbers. The circuitry also limits EMI and harmonic currents to tolerable levels, and enables flicker to be controlled.

POWER CONTROL CIRCUIT FOR THE HEATING
ELEMENT OF AN ELECTROPHOTOGRAPHIC DEVICE

FIELD OF INVENTION

The invention generally relates to power control systems and more particularly to a method and apparatus for enabling the power to a heating element in a device such as an electrophotographic copier or printer to be closely controlled while complying with power quality regulations.

10   ## BACKGROUND OF INVENTION

Electrophotographic printers and copiers produce an image by using dry toner. As part of the printing process, toner is fused onto a piece of paper or other medium using a heating element such as a high power halogen, tungsten or quartz lamp. The fuser lamp increases the temperature of the paper until the melting point of the toner is reached thereby enabling the toner to fuse to the paper in the desired image.

The resistance of the typical fuser lamp used in many electrophotographic printers and copiers varies greatly depending upon the temperature of the fuser lamp itself. When cold, the fuser lamp has a very low resistance, e.g., in the range of approximately 1 – 4 ohms. When hot, the resistance of the fuser lamp increases significantly, e.g., up to about 40

20   ohms. In short, the resistance of the fuser lamp can vary by a factor of about 6 - 12 over the typical operating temperature range of the lamp.

Consequently, a high amount of current may be drawn from the commercial power grid by the fuser lamp during the warm-up process. This can create significant

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voltage fluctuations on the power lines, which in turn may result in the visible perception of lights flickering. Recently, legislation has been enacted in various European jurisdictions to limit voltage fluctuations on the power lines and the resulting flicker. In addition to this, manufacturers of electrophotographic devices must often meet limits on the harmonic currents introduced onto power lines as well as conducted electromagnetic interference (EMI). See, for example, International Electrical Commission (IEC) regulation no. EN61000-3-2 for harmonic current limits, IEC regulation no. EN61000-3-3 for flicker, and CISPR B regulations for conducted and radiated EMI limits.

10   It will also be appreciated that the voltage provided by commercial power sources will vary depending upon the country in which the electrophotographic copier or printer is used. Since the resistance of the fuser lamp is fixed (or more accurately varies over a fixed range), its power consumption, which typically represents a major component of the power consumption of the copier or printer, will vary depending upon the power line voltage. For manufacturers of such devices, it is economically desirable to manufacture devices which operate universally on commercially available power supply systems throughout the world.

Furthermore, it is often desirable to control and vary the temperature of the fuser lamp in response to operating requirements. For instance, the heat output required of the fuser lamp will vary depending upon how fast paper or other print medium is flowing

20   through the electrophotographic copier or printer. The faster the paper flow, the greater the heat output required in order to properly fuse the toner thereon. The type of medium, e.g., quality of paper, also plays a factor. In addition, the relative humidity of the ambient environment also determines how much the heat the fuser lamp must produce since a more

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humid environment means that a greater amount of water is, absorbed by the print media which affects how fast it heats up.

For all of the foregoing reasons it is desirable to control the power flow to the fuser lamp in an electrophotographic copier or printer. It is also desirable to control the power flow so as not to be deleterious or destructive to the fuser lamp itself or drive components.

The prior art has attempted to overcome some of these problems, with limited success. For example, US Patent No. 4,928,055 to Kaieda et al. discloses complex circuitry for measuring the voltage and frequency of the power lines connected to an image forming

10   device. Based on this data, the circuitry determines the duration of time power should be applied to a heating element so that a predetermined amount of power is applied thereto irrespective of the power source. The circuitry controls the conduction angle of a triac. While the '055 patent is not particularly concerned with regulation of flicker, the circuitry thereof can be adapted to control flicker with a suitable temperature control algorithm such as disclosed in U.S. Patent No. 5,811,764 to Hirst. The circuitry of the '055 patent, however, is relatively expensive and does not adequately provide control of harmonic currents and conducted EMI.

U.S. Patent No. 5,789,273 to Hirst discloses an alternative technique for controlling the power applied to a resistive heating element such as a tungsten filament. In

20   this technique, a full wave rectifier rectifies the alternating current (AC) of the commercial power supply. A current smoothing inductor is connected to the positive terminal of the full-wave rectifier and the filament is connected to the inductor. A power switch is connected between the filament and a negative terminal of the rectifier. A capacitor is connected

between the inductor and the negative terminal of the rectifier. The switch is pulse width modulated (PWM) and thus switches the filament into and out of the circuit. When the filament is switched into the circuit, the capacitor discharges into the filament. When the filament is switched out of the circuit the input inductor charges up the capacitor and the process is repeated so as to prevent resonance in the LC tank formed by the inductor and capacitor. By varying the duty cycle, the effective resistance of the filament can be controlled thereby controlling the amount of power supplied thereto. Flicker can also be limited by slowly ramping up the duty cycle when the filament is cold. However, the primary problem with this circuit is that, depending on the type of fuser lamp employed, the

10 circuit may affect the life of a fuser lamp. In particular, note that in the '273 circuit a large effective direct current (DC) is applied to the filament. For many filaments the application of DC power results in black deposits which reduce the intensity of the heat output and hence the life of the filament. In some cases these deposits may result in a shortening on the filament life by half.

SUMMARY OF INVENTION

The invention seeks to provide a power circuit for enabling the power to a heating element such as a fuser lamp to be controlled whilst avoiding various of the limitations of the prior art. By providing a circuit for regulating power flow, the invention

20 also enables flicker to be controlled. The invention also seeks to provide a power circuit that produces acceptable harmonic currents and EMI noise.

According to one aspect of the invention a power circuit is provided comprising: an input filter connectable to an AC power source; an AC switch connected between the input filter and the heating element so as to enable the selective application of AC power to the heating element; and control circuitry connected to the AC switch for turning the AC switch on and off. A PWM switching technique is preferably used in order to enable the power applied to the heating element to be regulated.

The heating element of the electrophotographic device is characterized electrically as a parasitic inductance in series with a resistance that varies depending on the temperature of the heating element. The power circuit preferably includes circuitry for 10 periodically dissipating at least a portion of the energy stored in this parasitic inductance through a resistance which varies depending upon the amount of energy stored in the parasitic inductance.

In the embodiment of the power circuit described in detail herein, the energy dissipating circuitry includes a capacitor for receiving energy from the parasitic inductance and a first resistor for dissipating the energy stored in the capacitor, the first resistor thereby providing a first discharge path. A second discharge path, having a lower resistance than the first path, is also included for dissipating the energy stored in this capacitor. The second discharge path includes a switch which is turned on to activate the second path when the voltage across the capacitor exceeds a predetermined level. This level is selected to coincide 20 with an excess amount of energy arising out of high currents present during transient conditions, which the lower resistance of the second discharge path can dissipate at a greater rate than the first path.

In the embodiment described herein the power circuit also measures the quantity of electric charge flowing through the second discharge path and generates an output signal indicative of a short circuit condition when the charge exceeds a predetermined limit. This output signal can be used to turn the AC switch off. The power circuit also limits the peak current flow through the heating element to a predetermined maximum level.

In the embodiment described herein, the input filter is formed from an inductor connected to a first terminal of the AC power source and a capacitor connected to the inductor and a second terminal of the AC power source. The components of the input filter are selected to provide a low pass filter having a cut-off frequency that is higher than an operating frequency of the AC power source. The control circuitry pulse width modulates the AC switch at a PWM frequency higher than the cut-off frequency. For acceptable control of harmonic currents, the cut-off frequency is about 7 kHz and the PWM switching frequency is about 17kHz.

BRIEF DESCRIPTION OF DRAWINGS

The foregoing and other aspects of the invention will become more apparent from the following description of illustrative embodiments thereof and the accompanying drawings which illustrate, by way of example only, the principles of the invention. In the drawings, where like elements feature like reference numerals (which may bear unique alphabetical suffixes in order to identify specific instances of like elements):

Fig. 1 is a partly circuit, partly block diagram of a circuit for powering a fuser lamp according to one embodiment of the invention;

Fig. 2 is a circuit diagram showing an active voltage limiting block of the power circuit in greater detail;

Fig. 3 is a waveform diagram showing the current generated by the power circuit across the fuser lamp;

Figure 4 is a graph showing the characteristics of a non-linear inductor employed in the power circuit; and

Fig. 5 is a circuit diagram showing a peak current control block of the power circuit in greater detail.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENT

Fig. 1 shows a diagram of a power circuit 20 according to one embodiment of the invention. Note that in Fig. 1 certain portions of the circuit 20 are shown in system block diagram form. The input to the circuit 20 is a voltage source V_{LINE} which represents the commercial power source connectable to the circuit 20. In the illustrated embodiment the circuit 20 is designed to work with at least a 115 to 230 volt, 50 – 60 Hz, AC source.

An inductor L_1 is connected to the positive side of the power source. A capacitor C_1 is connected between the inductor and a ground point (as defined by the negative side of the power source). The inductor L_1 and capacitor C_1 together provide a low pass filter. In the illustrated embodiment the cut off frequency of the low pass filter is about 7 kilohertz as provided by a 150 µH inductor and 3.3 µF capacitor.

The circuit 20 features a bi-directional AC switch for enabling the controlled application of power to a fuser lamp 26. In the illustrated embodiment the AC switch is formed from two power transistors Q1 and Q2 (preferably IGBTs), each of which has a co-

packed anti-parallel diode associated therewith. Between Q1 and Q2 two sense resistors R_{SEN1} and R_{SEN2} are connected as shown. The sense resistors have very low resistances, for example 10-20 mΩ each, and a reference point 28 is defined between the two sensor resistors. The usage of the sense resistors is described in greater detail below.

The circuit elements of the fuser lamp 26 include a parasitic inductance L_{LAMP} in series with a resistance R_{LAMP}. The inductance L_{LAMP} arises from the filament of the lamp itself as well as the wiring used to connect the lamp 26 with the remaining portions of the circuit. In a photocopier, for instance, this may involve over a meter of wiring. The lamp resistance R_{LAMP} varies depending upon the temperature of the lamp itself, as previously

10   described. As noted above, the resistance of the fuser lamp 26 can vary by a factor of about 6 - 12 over the typical operating temperature range of the lamp.

The filtered AC voltage present at node 24 is "chopped" by the AC switch. More particularly, the power transistors Q1 and Q2 are pulse width modulated (PWM) at a rate of approximately 17 kilohertz and thus a PWM AC voltage is applied to the fuser lamp 26. The duty cycle for the PWM switching is controlled by an input signal V_{IN} that is generated by a power controller 70 discussed in greater detail below. V_{IN} is fed to a PWM generator 30, as known in the art *per se*, which produces a 17 kHz square wave pulse having a duty cycle corresponding to that represented by the magnitude of V_{IN}. (A linear relationship may be used wherein, for example, $V_{IN} = 5V$ yields a 100% duty cycle and $V_{IN} = 0V$ yields

20   a 0% duty cycle.) An opto-coupler 32 provides electrical isolation between the low power circuitry associated with controller 70 and the high power circuitry associated with the remainder of circuit 20. As explained in greater detail below, the output of the opto-coupler 32 feeds a gate drive circuit 34 as known in the art *per se* which translates the PWM

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generator to the appropriate voltage and current levels required to drive the gates of Q1 and Q2. Given the polarities or channel characteristics of Q1 and Q2, as shown, transistor Q1 is on or conducts during the on-duty portion of the PWM cycle when the AC voltage at node 24 is positive, and Q2 conducts through its anti-parallel diode during this period. Transistor Q2 is on or conducts during the on-duty portion of the PWM cycle when the AC voltage at node 24 is negative, and transistor Q1 conducts through its anti parallel diode during this period. During the off-duty portion of the PWM cycle both transistors Q1 and Q2 are off or do not conduct, so substantially no current will flow through Q1 and Q2 during these periods.

During the on-duty portion of the PWM cycle the parasitic inductance L_{LAMP}

10 of the fuser lamp 26 charges up. The quantum of energy stored is $½•L_{LAMP}•i^2$. During the off-duty portion of the PWM cycle this parasitic inductance causes large voltage spikes on Q1 and Q2 every time they are turned off. These spikes must be controlled in order to limit EMI emissions. For this reason an EMI snubber 38 consisting of a capacitor C_{SNB} in series with a resistor R_{SNB} is disposed in parallel with each transistor Q1 or Q2, in order to limit the dv/dt rate, as well known in the art.

In addition, a path must be provided to dissipate the energy stored in the parasitic inductance L_{LAMP} as well as to prevent transistor breakdown. This is provided by a dissipative voltage clamp 40 which absorbs and dissipates the energy stored in L_{LAMP} during the off-duty portion of the PWM cycle. More particularly, the clamp 40 comprises

20 capacitors C_{CL1} and C_{CL2} each of which is connected in parallel with a resistor R_{CL1} or R_{CL2}. As soon as the off-duty portion of the PWM cycle begins the energy stored in L_{LAMP} flows to the clamping capacitors (C_{CL1} and C_{CL2} are essentially connected in parallel as will be described shortly) and charges them up. Blocking diodes D_{CL1} or D_{CL2} prevent current flow

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to node 24. During the on-portion of the PWM cycle the transistors Q1 and Q2 are switched on enabling current flow therethrough. This path presents a substantially smaller resistance than the dissipative voltage clamp 40, so substantially no current will flow to the clamp 40 from the power source. This enables the clamping capacitors C_{CL1} and C_{CL2} to discharge through the dissipative resistors R_{CL1} and R_{CL2} during the on-portion of the PWM cycle. The time constant formed by the clamping capacitors and dissaptive resistors is selected to enable the cyclical charging and discharging of the capacitors over the range of duty cycle ratios the circuit 20 is designed to operate over without allowing any excessive voltages to develop as a result of resonant conditions. Illustrative values for the clamping capacitors and dissapitive

10   resistors are 4.4 μF and 39KΩ for a 17kHz PWM frequency.

The power circuit 20 further includes an active voltage-limiting block 50 that is connected to the dissipative voltage clamp 40 and reference node 28. The block 50 functions to limit the voltage across the clamping capacitors C_{CL1}, C_{CL2} and transistors Q1, Q2 by introducing another, lower resistance, discharge path for the clamping capacitors. This additional path is engaged or reacts only under transient conditions when the current through the fuser lamp 26 is very high resulting in the clamping capacitors being charged above a predetermined value. For instance, when the fuser lamp 26 is cold the inrush current (depending on the specific resistance characteristics of the device) can reach 40 Amps, as compared to say 12 Amps when the lamp 26 has reached operating temperature. This inrush

20   current is about 3 times higher than the steady state current, whereby 9 times as much energy is stored in the clamping capacitors at startup. A more drastic situation will exist in the event of a short circuit condition. In order to dissipate the extra energy in the same amount of time, a considerably lower-valued resistor is required, which is provided by the additional

conductive path in block 50. However, this additional conductive path is not engaged during non-transient periods since the power loss would otherwise be too great during steady state conditions.

Fig. 2 shows the circuitry within the active voltage-limiting block 50 in greater detail. Note also that in Fig. 2 the capacitors C_{CL1}, C_{CL2} and resistors R_{CL1}, R_{CL2} of clamp 40 are shown connected in parallel at node 28. This is an equivalent circuit from a practical point of view since the voltage drop across the sense resistors R_{SEN1} and R_{SEN2} is negligible and thus presents an alternative embodiment (although the configuration shown in Fig. 1 is preferred since it results in less noise across the sense resistors).

10   Referring specifically to Fig. 2, the active voltage-limiting block 50 comprises resistors R_{D1} and R_{D2} which form a resistor divider leg. The voltage at node 52 of the resistor divider leg is compared by a hysteresis comparator 54 (comprising feedback resistors $\frac{R_1}{R_f}$) against a reference voltage V_{ref}. The values of the resistors and V_{ref} are selected so as to trigger the hysteresis comparator 54 to generate a gate driving signal 56 when the voltage across the clamp 40 reaches a predetermined value deemed to represent transient conditions. In the illustrative embodiment, this value is set to 470 V, which is believed sufficient to enable the power circuit 20 to operate over a wide input voltage range. The gate-driving signal activates a switch such as MOSFET Q3. Activating the switch Q3 enables the clamping capacitors to discharge through a low-valued (e.g., 750Ω) power resistor R_T which

20   permits a much higher current flow therethrough than $R_{CL1}||R_{CL2}$. The hysteresis comparator 54 operates to turn off the transistor Q3 when the voltage across the clamping capacitor

returns to 400V. This minimizes the switching frequency of Q3 and thereby minimizes the EMI noise and switching losses associated with Q3.

In the event the power circuit 20 is not enclosed within a metal chassis, another problem that a designer may have to overcome is limiting the radiated EMI noise. This noise is caused in part by the speed of the AC switch which results in a high dv/dt rate. This problem is solved by the EMI snubbers 38. However, another source of radiated EMI noise arises from a high di/dt rate caused by the PWM switching of the AC voltage at node 24. The current wave form is shown in Fig. 3. Under some conditions the parasitic inductance of the fuser lamp 26 may be sufficient to limit the slope 27 (i.e., rise and fall 10 times) of the current wave form, and hence the di/dt rate, to a point where the radiated EMI noise is tolerable. However, the parasitic inductance L_{LAMP} may be insufficient for this purpose. For instance, it was found that a 5µH parasitic inductance was insufficient to limit radiated EMI in the illustrated embodiment. In order to overcome this problem an additional inductor L4 (shown in phantom in Figs. 1 & 2) was installed in series with the fuser lamp 26 in order to lessen the current slope. This additional inductor L4 adds to the overvoltage problem caused by the parasitic inductance L_{LAMP}, but as mentioned previously this problem is dealt with by the dissipative voltage clamp 40 and the voltage-limiting block 50. In order to minimize the effect of L4, a non-linear inductor having the inductance characteristics shown in Fig. 4 was selected. Note that at a relatively high current of 40A L4 has an 20 inductance of about 5µH and at about 12A an inductance of about 10µH. These characteristics help to reduce overvoltage conditions during transient conditions, where radiant EMI is only momentarily generated, but ensure that sufficient inductance is present in

steady state conditions, where overvoltage is not an issue, to limit radiated EMI to tolerable levels.

To further constrain overvoltage conditions the power circuit 20 includes a block 62, shown in greater detail in Fig. 5, which functions to limit the peak current through the AC switch (Q1 and Q2) and fuser lamp 26 to a predetermined level, e.g., 40 Amps. The resistors R_{SEN1} and R_{SEN2} are used to sense the current through the AC switch, R_{SEN1} being employed when the AC voltage is positive and R_{SEN2} being employed when the AC voltage is negative. Each sensor is associated with a level comparator 63 and a latch 64. When the voltage drop across R_{SEN1} or R_{SEN2} exceeds a predetermined level (about 0.7V in the

10   illustrated embodiment), the corresponding comparator 63 generates a voltage equivalent to a boolean or binary 1; otherwise the comparator 63 generates a voltage equivalent to binary 0. When the output of the comparator 63 goes high, the corresponding latch 64 is set and generates a binary 1 output. The latch 64 will remain this way until reset. The output of the latches 64 are fed into a NOR gate 65 such that whenever the predetermined peak current is sensed (whether the AC voltage is positive or negative) the output of the NOR gate 65 is a binary 0. The output of the NOR gate 65 is one of the inputs to an AND gate 66. The other input to the AND gate 66 is the PWM signal from the opto-coupler 32. Thus, whenever the current through the AC switch exceeds the predetermined peak limit, the foregoing logic forces the PWM signal to 0 resulting in the AC switch being turned off so as to decrease the

20   current flow.

The latches 64 are reset by the PWM signal itself. In this manner the peak current control block 62 operates on a per PWM cycle-by-cycle basis. This prevents excess switching from a current and increases the stability of circuit.

Referring now to Fig. 2, the active voltage limiting block 50 also provides short circuit protection 58. This is carried out by measuring how much electric charge flows through the alternative discharge path. More specifically, note that in every PWM cycle the clamping capacitors $C_{CL1} \| C_{CL2}$ discharge so that under normal operating conditions the voltage thereacross should reach a maximum limit at 100% duty cycle. However in a short circuit condition a very high current will pass through the fuser lamp 26 and the clamping capacitors will be charged to a voltage exceeding this maximum limit. Structurally, the short circuit protection is provided by a capacitor C_{SC} that charges up whenever the low resistance discharge path is active or conducts. Resistor R_{SC1} is selected so as not to

10 substantially affect the resistance of the alternative discharge path. In conjunction, the values of R_{SC2} and C_{SC} are selected to enable the capacitor to charge to a predetermined voltage level V_{ref2} that would not ordinary be reached unless the alternative discharge path is active for a relatively extended period of time. The voltage at C_{SC} is fed into a second comparator 56 and measured against V_{ref2}. When this voltage level is reached the comparator 56 generates a shut-off signal 60 that may be used to inhibit the PWM function (i.e., generate a zero duty cycle).

The power circuit 20 makes it possible for the controller 70 control the duty cycle in order to provide a desired heat output. The desired heat output may be based on factors such as the type of print medium, its speed through the electrophotographic device,

20 and the desired temperature of the print medium for proper printing. The power controller 70 can measure the temperature of the fuser lamp (sensing circuitry not shown) and employ or implement a compensator as well known in the art to minimize any error between the desired and measured heat output of the fuser lamp. The controller 70 may also include logic for

slowly (e.g., over a period of 1-2 seconds) ramping up the duty cycle when the fuser lamp is cold in order to prevent a large inrush current, to thereby control flicker. Suitable algorithms for controlling flicker are known in the art and may be implemented by the controller 70 for this purpose.

Note also from the foregoing that the power circuit 20 applies an AC voltage to the fuser lamp 26. In this manner, the potentially destructive effects of a DC voltage are eliminated. Moreover, despite the direct application of AC voltage to the fuser lamp 26, conducted and radiated EMI is controlled by the EMI snubbers 38, clamp 40 and if necessary, L4. Harmonic currents are also adequately controlled since the relatively high

10   frequency PWM switching of the transistors Q1 and Q2 yield harmonic currents that are multiples of the switching frequency (e.g., multiples of 17kHz). These harmonic currents are blocked or filtered by the input filter formed from L_1 and C_1. Due to the relatively high frequencies involved, these components may be relatively small and inexpensive.

Those skilled in the art will understand that while the AC switch described herein has been formed from two IGBT transistors the AC switch can in the alternative be formed from a single device or by different types of transistors. The IGBTs are preferred for their power handling capabilities and relatively low costs. In addition, while two discharge paths have been shown for the clamping capacitors, it should be understood that in the alternative more than two discharge path can be employed, or a single discharge paths having

20   a controllable resistance can be employed. The illustrated embodiment, however, is believed to be the most-cost effective technique. Furthermore, while the power circuit described herein has employed a fixed PWM switching frequency and a variable PWM duty cycle to control the power applied to the heating element, those skilled in the art will appreciate that

the off-time of the AC switch may be fixed while the switching frequency is varied. A combination of both techniques may also be applied. Similarly, those skilled in the art will understand that numerous modifications and variations may be made to the embodiments described herein without departing from the spirit of the invention.

CLAIMS

1. A power circuit for control of a heating element, comprising:

an input filter connectable to an AC power source;

an AC switch connected between the input filter and the heating element so as to enable the selective application of AC power to the heating element; and

control circuitry connected to the AC switch for turning said switch on and off in order to enable the amount of power applied to the heating element to be regulated.

2. The power circuit according to claim 1, wherein the heating element comprises a parasitic inductance in series with a resistance which varies depending on the temperature of the heating element.

3. The power circuit according to claim 2, including circuitry for periodically dissipating at least a portion of the energy stored in said parasitic inductance through a resistance which varies depending upon the amount of energy stored in the parasitic inductance.

4. The power circuit according to claim 3, including an inductor connected in series with the AC switch and the heating element, wherein said energy dissipating circuitry is operative to dissipate at least a portion of the energy stored in the inductor and said resistance varies depending upon the total amount of energy stored in the parasitic inductance.

5. The power circuit according to claim 3, wherein said energy dissipating circuitry includes a capacitor for receiving energy from said parasitic inductance and a first resistor for dissipating the energy stored in the capacitor, the first resistor thereby providing a first discharge path.

6. The power circuit according to claim 5, including:

a second discharge path for dissipating the energy stored in said capacitor, the second discharge path being activatable and when activated having a lower resistance than the first path;

a switch disposed in the second discharge path; and

voltage limiting circuitry for turning on the switch, and thereby activating the second discharge path, when the voltage across the capacitor exceeds a predetermined level.

7.   The power circuit according to claim 6, further including circuitry connected to the second discharge path for measuring the quantity of electric charge flowing through the second discharge path and generating an output signal indicative of a short circuit condition when said charge exceeds a predetermined limit.

8.   The power circuit according to claim 7, including circuitry for limiting the current flow through the heating element to a predetermined level.

9.   The power circuit according to claim 8, wherein the input filter comprises an inductor connectable to a first terminal of the AC power source and a capacitor connected to the inductor and a second terminal of the AC power source.

10.   The power circuit according to claim 9, wherein:

the input filter is a low pass filter having a cut-off frequency that is higher than an operating frequency of the AC power source; and

the control circuitry pulse width modulates the AC switch at a PWM frequency higher than the cut-off frequency.

11.   The power circuit according to claim 10, wherein the cut-off frequency is about 7 kHz and the PWM switching frequency is about 17kHz.

12.   The power circuit according to claim 10, wherein the control circuitry varies the duty ratio of the PWM cycle or the PWM switching frequency in accordance with a control signal.

13.   The power circuit according to claim 12, further including a power controller for measuring the temperature of the heating element and generating said control signal so as to minimize any error between the measured temperature of the heating element and a desired value therefor.

14.   The power circuit according to claim 1, wherein the input filter comprises an inductor connectable to a first terminal of the AC power source and a capacitor connected to the inductor and a second terminal of the AC power source.

15.   The power circuit according to claim 14, wherein:
the input filter is a low pass filter having a cut-off frequency that is higher than an operating frequency of the AC power source; and
the control circuitry pulse width modulates the AC switch at a PWM frequency higher than the cut-off frequency.

16.   The power circuit according to claim 15, wherein the cut-off frequency is about 7 kHz and the PWM switching frequency is about 17kHz.

17.   The power circuit according to claim 15, wherein the control circuitry varies the duty ratio of the PWM cycle or the PWM switching frequency in accordance with a control signal.

18.   The power circuit according to claim 17, further including a power controller for measuring the temperature of the heating element and generating said control signal so as to minimize any error between the measured temperature of the heating element and a desired value therefor.

19.   A method of controlling a heating element having a parasitic inductance in series with a resistance which varies depending on the temperature of the heating element, the method comprising:

filtering an AC power source with a low pass filter;

periodically applying the filtered AC power to the heating element for relatively small periods of time;

periodically dissipating at least a portion of the energy stored in the parasitic inductance through a resistance, wherein the resistance varies depending on the amount of energy stored in the parasitic inductance.

20.   The method according to claim 19, including the step of reducing the slope of current waveforms arising out of the periodic application of the AC power to the heating element.

21.   The method according to claim 19, wherein the step of periodically dissipating at least a portion of the energy stored in the parasitic inductance includes:

absorbing said portion of energy stored in the parasitic inductance during time periods when no AC power is applied to the heating element;

dissipating said absorbed energy through a first discharge path; and

in the event the absorbed energy exceeds a predetermined level, additionally dissipating the excess absorbed energy through a second discharge path having a lower resistance than the first discharge path.

22.   The method according to claim 21, wherein the heating element is a fuser lamp employed in an electrophotographic device.

23.   The method according to claim 22, further including measuring the quantity of electric charge flowing through the second discharge path and generating an output signal indicative of a short circuit condition when said charge exceeds a predetermined limit.

24.   The method according to claim 22, including limiting the peak current flow through the heating element to a predetermined limit.

25.   The method according to claim 22, wherein the step of filtering the AC power source is provided by connecting an inductor to a first terminal of the AC power source and connecting a capacitor to the inductor and a second terminal of the AC power source.

26.   The method according to claim 22, wherein:

the low pass filter has a cut-off frequency that is higher than an operating frequency of the AC power source, and

an AC switch is connected to the heating element for enabling the periodic application of power thereto, said AC switch being pulse width modulated at a PWM frequency higher than the cut-off frequency.

27.   The method according to claim 26, wherein the cut-off frequency is about 7 kHz and the PWM switching frequency is about 17kHz.
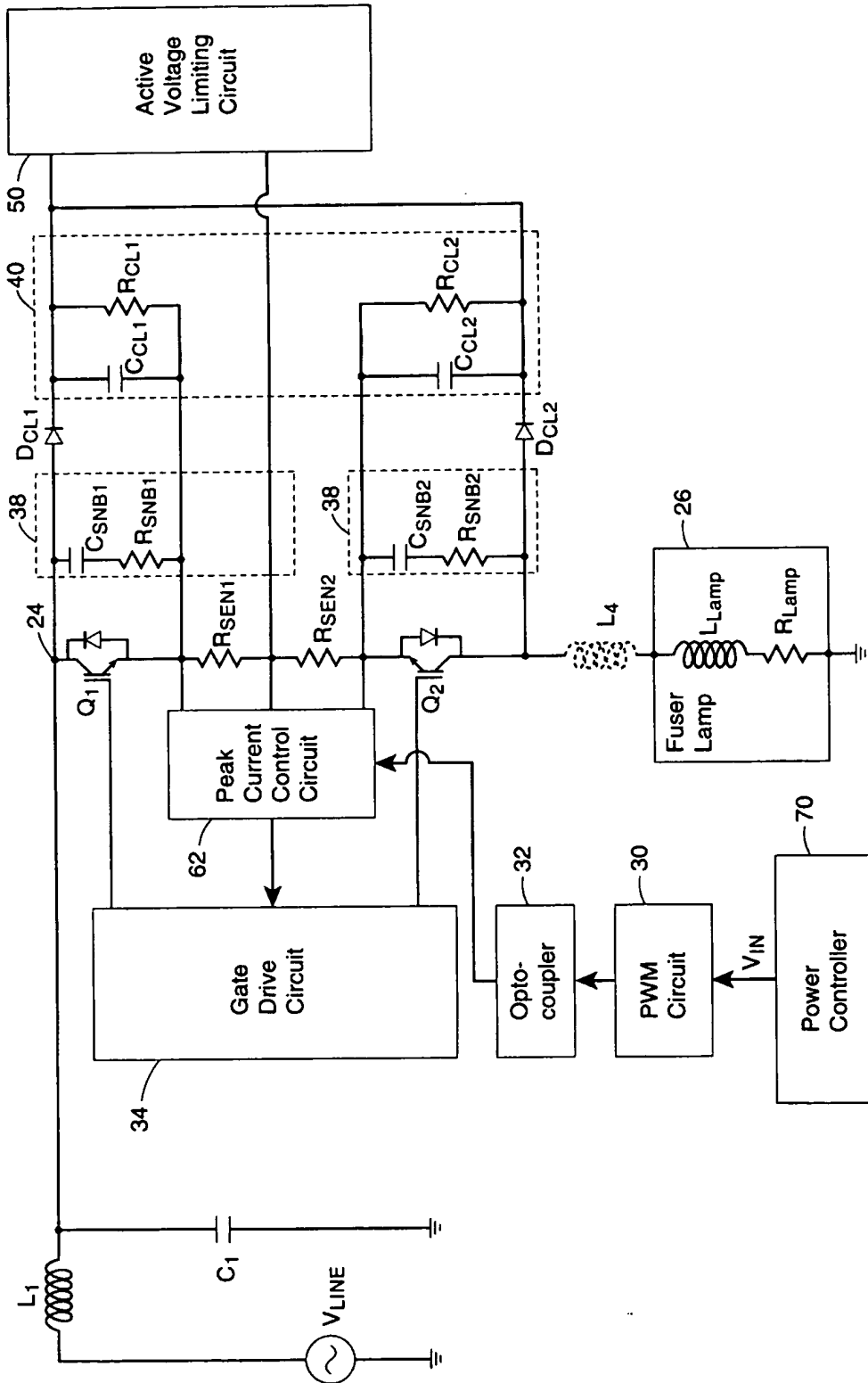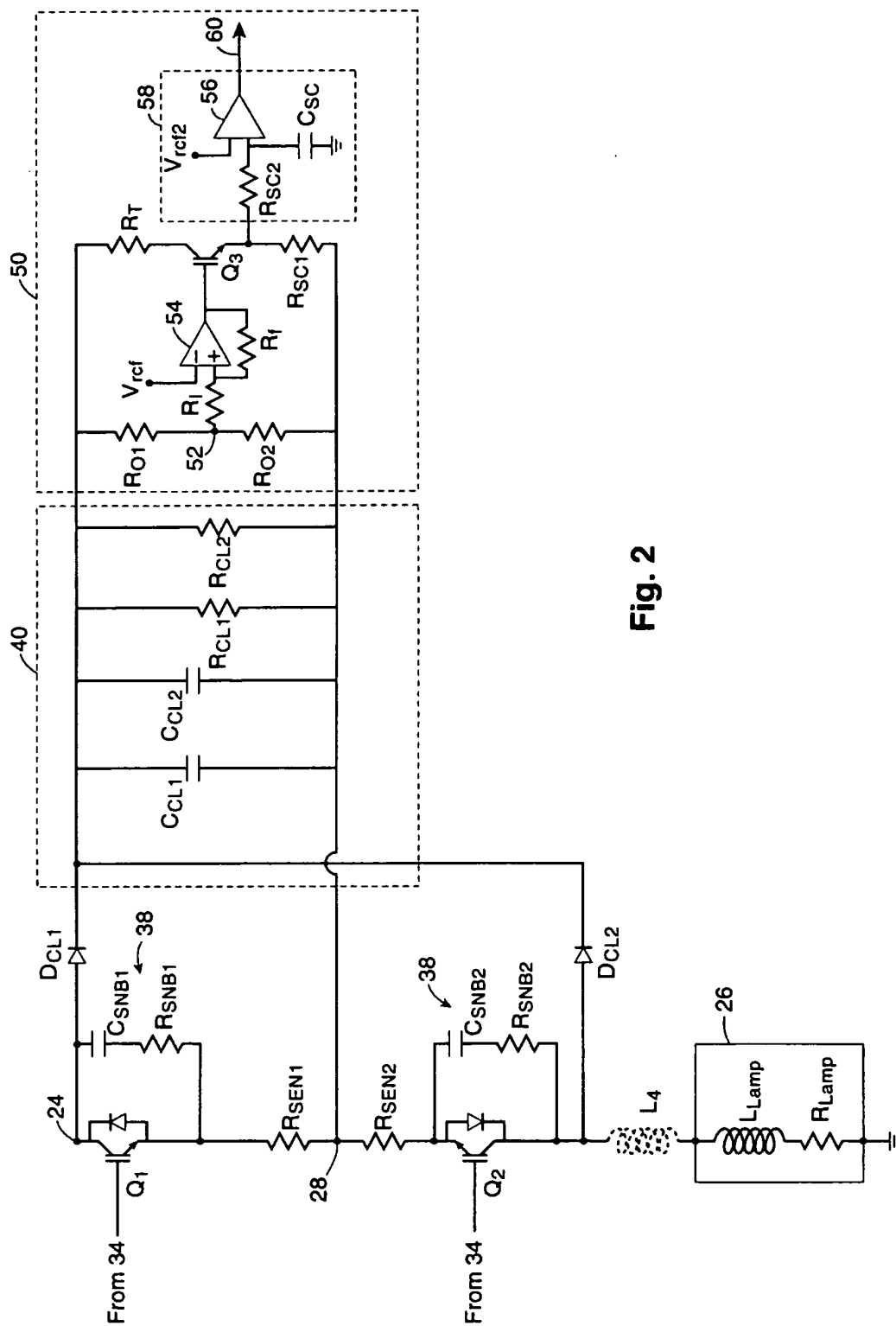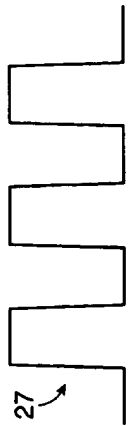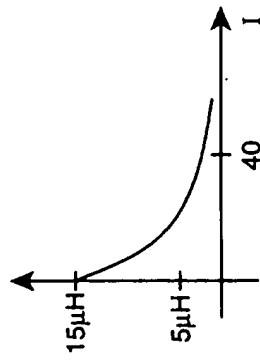
Fig. 1

Fig. 2

Fig. 5

Fig. 3
(not to scale)

Fig. 4

Active Voltage Limiting Circuit — 50

40

R_{CL1}
C_{CL1}
R_{CL2}
C_{CL2}

D_{CL1}
D_{CL2}

38

C_{SNB1} R_{SNB1}
C_{SNB2} R_{SNB2}

26

24

R_{SEN1} R_{SEN2}

L_4

L_{Lamp} R_{Lamp}

Fuser Lamp

Q_1 Q_2

Peak Current Control Circuit

62

Gate Drive Circuit

34

Opto-coupler 32

PWM Circuit 30

V_{IN}

Power Controller 70

L_1

C_1

V_{LINE}